REMARKS

The Office Action mailed on February 26, 2002 has been received and reviewed.

Claims 1 through 20 are currently pending in the application.

Claims 1 through 15 are withdrawn from consideration as being directed to a non-elected invention.

Claims 16 through 20 stand rejected. Claim 21 is a newly submitted claim.

Reconsideration of the above-referenced application is respectfully requested.

Objections to the Specification

The title was objected to as being non-descriptive (Office Action, item 2, page 2). Appropriate correction has been made and revised drawings submitted for Examiner's approval.

Objections to the Drawings

The corrected and substitute drawings submitted on November 29, 2001 was objected to as failing to comply with 37 CFR 1.84(p)(5) (Office Action, item 4, page 3). Appropriate correction has been made.

35 U.S.C. § 102(b) Anticipation Rejections

Claims 16 through 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Deguchi (JP 62-18714, hereinafter "Deguchi"). Applicants have obtained a translation of Deguchi and are submitting that information on a separate IDS pursuant to 37 C.F.R. §97(c)(1).

Deguchi relates to a method for forming alignment marks in semiconductors using dry etching methods to form finely localized roughened areas, said marks having a part with high light reflectance and another part having low light reflectance, wherein positioning control of the substrate on which these parts are formed is performed by detecting the reflected light from both of [illegible] Deguchi, claim, page 2). More specifically, fine square conical projections as shown

[illegible] page 4 of numerous fine cone shaped crystal products are formed as shown in Fig. [illegible]

by use of dry etching by high-frequency glow discharge using a mixed gas of CF_4 and O_2 (*Id.*, lines 28-31, page 4).

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

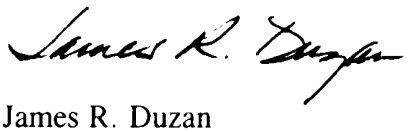
Applicants respectfully submit that Deguchi does not anticipate the instant invention recited in independent claim 16 because each and every element as set forth therein is not found, either expressly or inherently described in Deguchi. In particular, Deguchi does not teach or disclose overlay targets with a series of raised lines. Rather, as summarized hereinabove, Deguchi only teaches and discloses alignment marks or dry-etched localized roughened areas characterized by either fine square conical projections or numerous fine rod-shaped crystal protrudes, depending on the dry etching manufacturing technique used. Thus, Deguchi does not anticipate claim 16.

Further, claims 17 through 21 are allowable, among other reasons, as depending either directly or indirectly from independent claim 16, which is allowable.

Applicants further submit that Deguchi does not anticipate the invention recited in claims 17 and 18 wherein the semiconductor substrate is selected from a group consisting of silicon, gallium and sapphire substrates. Also, Deguchi does not anticipate the invention recited in the newly submitted claim 21, wherein the etching process of claim 16 is a wet etching process.

Therefore, Applicants respectfully request that the anticipation rejection under 35 U.S.C. § 102(b) of claims 16 through 20 be withdrawn, the claims allowed, and the case passed to issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made
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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Please amend the title as follows: [Residue Free] Raised-lines Overlay Semiconductor Targets and Method of Making the Same.

IN THE SPECIFICATION:

[0005] Known overlay targets generally include a pattern formed by one or more etched trenches or pad areas. Illustrated in drawing FIG. 1 is a portion of an intermediate wafer structure 5 including a simple trench-type overlay target 10. The overlay target 10 includes a continuous rectangular trench 11 [12] etched into the semiconductor substrate 14 outside the chip pattern 15 [16]. Of course, the overlay target depicted in drawing FIG. 1 is provided for illustrative purposes only. It is understood that overlay targets can be created using a variety of patterns formed from continuous trenches, discontinuous trenches, or pad areas.

[0006] Depicted in drawing FIG. 2 is a cross section taken at line A-A of drawing FIG. 1, illustrating [and illustrates] an overlying material layer 16 deposited over the surface 18 of the semiconductor substrate 14 after formation of the trench 11 defining the overlay target. As can be seen in drawing FIG. 2. the overlying material layer 16 tends to conform to the topography created by the trench 11. Such conformation results in the formation of depressions 20 at the upper surface 22 of the overlying material layer 16. Even after a polishing step, portions 24 (shown in drawing FIG. 3) of the depressions 20 may still remain and serve as collection points for process residue 26, such as hemispherical grain ("HSG") Poly. As is shown in drawing FIG. 4, because the residue 26 overlies the trench 11 defining overlay target 10, the residue 26 works to obscure the outlines (depicted by dashed lines 28a and 28b) of the pattern formed by the trench 11, making the outlines 28a[,] and 28b of the overlay target 10 to appear ragged or inconsistent. Though [drawing FIG. 2 through drawing FIG. 4 depict features associated with a trench type overlay